REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for indicating that claims 17-23, 29-35, and 41-47 contain allowable subject matter. Further, Applicant thanks the Examiner for the courtesies extended in the Examiner Interview of May 16, 2005.

Disposition of Claims

Claims 1-47 are pending in the present application. Claims 1, 11, 12, 24, and 36 are independent. The remaining claims depend, directly or indirectly, from claims 1, 12, 24, and 36.

Claim Amendments

Independent claim 11 has been cancelled without prejudice or disclaimer. Further, claims 23, 35, and 47 have been amended to correct minor typographical errors. No new matter has been added by way of these amendments.

Rejection(s) under 35 U.S.C § 102

Claims 1-16, 24-28, and 36-40 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,680,636 issued to Parry *et al.* (hereinafter "Parry"). Independent claim 11 has been cancelled by way of this reply. Thus, the rejection is now moot with respect to claim 11. With respect to claims 1-10, 12-16, 24-28, and 36-40, this rejection is respectfully traversed for at least the reasons set forth below.

The present invention is directed to a technique that uses one or more biasable delay drivers to reduce clock grid skew in an integrated circuit (*see* Specification, abstract). The biasable delay drivers are capable of compensating for unbalanced loading and RC wire induced skew (*see* Specification, abstract). For example, referring to Figure 5a, in one embodiment of

the present invention, a global clock grid header (17) outputs a signal to two different loaded paths (92, 94). Each loaded path is subject to an RC load. However, the RC load of the first loaded path (92) is different from the RC load of the second loaded path (94). This unbalanced loading results in skew between the signal at the end of the first loaded path (shown as *y*) and the signal at the end of the second loaded path (shown as *z*). Therefore, biasable delay drivers (e.g., 104, 106, 108) are positioned at points on the first loaded path (92) and the second loaded path (94) (*see* Specification, Figure 5a; paragraph [0033]).

Figure 5c shows a biasable delay driver (130) in accordance with an embodiment of the present invention as shown in Figure 5a. The biasable delay driver is formed from a biasable delay NAND gate (132) and an inverter (134) of fixed size. The size of the NAND gate (132) (i.e., Wp and Wn, the widths of the PMOS and NMOS transistors, respectively) may be selectively sized, which corresponds to a change in the delay of the of the biasable delay driver (*see* Specification, paragraph [0035]).

By selectively sizing a biasable delay driver in accordance with one or more embodiments of the present invention, a fast path may be compensated for by slowing down the path (*i.e.*, the size of the biasable delay driver is reduced to slow down the path). Similarly, a slow path may be compensated for by selectively sizing the biasable delay driver (*i.e.*, sizing up the biasable delay driver) to speed up the path (*see* Specification, paragraph [0035]). Thus, any delay in the first loaded path (92) relative to the second loaded path (94) may be compensated for by using selectively sized biasable delay drivers at the end of each path (104, 106, 108). Similarly, if the second loaded path (94) is delayed relative to the first loaded path (92), this delay may be compensated for through the use of selectively sized biasable delay drivers at the end of each path (104, 106, 108).

Accordingly, claim 1 of the present invention requires selectively sizing a biasable delay driver based on a delay of a clock signal from a clock source to a point on a first path on which the clock signal propagates. Claim 24 requires instructions residing in a memory and executable by a processor for selectively sizing a first biasable delay driver depending on a first delay, wherein the first biasable delay driver inputs a clock signal at the point on a first path on which the clock signal propagates.

Parry, in contrast to the present invention, is directed to source synchronous multichip device implementations. Parry describes a clock edge placement circuit to adjust a clock signal to control synchronous sampling by external logic elements. In other words, the delay line of the clock edge placement circuit is adjusted to maintain the phase of the clock signal relative to data signals to control sampling by external logic (*see* Parry, col. 3, line 58 – col. 4, line 6).

Specifically, as discussed with reference to Figure 3 of Parry, a source chip (31) and a destination chip (32) of a multichip system (30) are connected via a series of data channels (36) and a clock channel (37) (*see* Parry, col. 6, lines 29-34). In system (30), the phase of the clock signal (38b) emerging from the clock circuit (35) is optimally adjusted with respect to *a different signal, i.e.*, the data signal. In other words, as described in Parry, the phase of the clock signal is adjusted such that "when the clock signal and data signals arrive at logic elements 34 of destination chip 32, the phase of the clock signal is adjusted such that the rising and falling edges of the clock signal are optimally placed (e.g., 1/4 clock cycle delay for optimal setup-and-hold times) with respect to the data signals." *See* Parry, col. 6, lines 574. Legends (38) and (39) describe the relative positions of the data signals (38A, 39A) and the clock signal (38B; 39B) before and after the synchronization (*see* Parry, col. 6, lines 64-65).

As discussed with reference to Figure 6 of Parry and discussed in the Examiner Interview of May 16, 2005, a clock edge placement circuit (60) according to Parry comprises a multi-tap delay line (66). The delay line (66) comprises a series of delay elements ("taps") arranged end-to-end such that each tap used adds an incremental amount of delay on the delay line (*see* Parry, col. 8, lines 20-24). The delay of the clock edge placement circuit is adjusted to control synchronous sampling by external logic elements, such as logic element (34) of Figure 3 of Parry (*see* Parry, col. 8, lines 33-36).

Figure 12 shows a delay stack (310) of Parry. Delay line (615) of delay stack (310) receives a signal, and similar to delay line (66) of Figure 6, includes a series of taps to control the delay of the signal. As seen in Figure 12 of Parry, each tap is formed by combining two inverters in series (*see* Parry, col. 12, lines 55-63). As further discussed with reference to Figure 12 of Parry, the inverters are fabricated to be as close to identical to each other as possible (*see* Parry, col. 12, line 64 – col. 13, line 1). Thus, each tap selected for use in the delay line (615) adds an incremental amount of delay identical to each of the other taps in the delay line (615).

The Examiner asserts that Parry teaches a first ***bi-stable*** delay driver that inputs a clock signal at a point on a first path, where the first bi-stable delay driver is selectively sized based on a delay of the clock signal from the clock source to the point on the first path. However, it is unclear as to how Parry teaches a bi-stable delay driver in view of the above. Further, it is clear to one skilled in the art that Parry does not teach, as required by claim 1 of the present invention, an integrated circuit having a clock source that outputs a clock signal, where the clock signal propagates down a first path, and a first ***biasable*** delay driver that inputs the clock signal at a point on the first path, where the first biasable delay driver is selectively sized based on a delay of the clock signal from the clock source to the point on the first path. Further, Applicant notes that this distinction between Parry and the claimed invention was discussed and

agreed to by the Examiner in the Examiner Interview of May 16, 2005. Accordingly, at least for this reason alone, the claimed invention is clearly patentable over Parry.

In view of the above, Parry fails to show or suggest the present invention as recited in amended independent claims 1 and 24. Independent claims 12 and 36 are directed to a method and computer readable medium, respectively, and were rejected for the same reasons as claims 1-11. Thus, amended independent claims 1, 12, 24, and 36 are patentable over Parry. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/166001; P7131).

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Respectfully submitted,

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